

AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs.

On pages 3-4, in paragraph [0009]:

In general, in one aspect, one or more embodiments of the present invention involve a ~~computer system comprising a reconfigurable cache memory, comprising a programmable memory unit;~~ a functional unit in communication with the cache ~~programmable-memory-unit~~, and a reconfiguration module. The functional unit executes applications using the the cache ~~programmable-memory-unit~~. The reconfiguration module is for determining an optimal configuration of the cache memory for a particular application and programming the cache ~~programmable-memory-unit~~ to the optimal configuration.

On page 4, in paragraph [0010]:

In general, in one aspect, one or more embodiments of the present invention involve a method of reconfiguring cache memory comprising determining an optimal configuration of the cache memory for a particular application executed by a functional unit using the cache a ~~programmable-memory-unit~~; and programming the cache ~~programmable-memory-unit~~ to the optimal configuration.

On page 4, in paragraph [0011]:

In general, in one aspect, one or more embodiments of the present invention involve a ~~reconfigurable cache memory computer system~~ comprising means for determining an optimal configuration of cache memory for a particular application executed by a functional unit using the cache a ~~programmable-memory-unit~~; and means for programming the cache ~~programmable~~ memory unit to the optimal configuration.

On page 4, in paragraph [0012]:

In general, in one aspect, one or more embodiments of the present invention involve a ~~computer system~~ reconfigurable cache comprising a field-programmable gate array, ~~[[;]]~~ a functional unit in communication with the field-programmable gate array, and a reconfiguration module. The functional unit executes applications using the field-programmable gate array. The reconfiguration module for determining an optimal configuration of the field-programmable gate array ~~memory~~ for a particular application and programming the field-programmable gate array to the optimal configuration. The reconfiguration module determines the optimal configuration by collecting performance information and analyzing the collected performance information.

On page 5, in paragraph [0022]:

The system (100) shown has a functional unit (102), a programmable memory ~~unit~~ module (104) such as a field-programmable gate array (FPGA) module, and a reconfiguration unit (106). The reconfiguration unit (106) controls the programmable memory ~~FPGA~~ module (104), which serves as the different caches (i.e., l1 cache, l2 cache, and l3 cache) necessary for operation. To set up the configuration of the programmable memory ~~FPGA~~ module (104), a vector is supplied from the reconfiguration unit (106).

On page 6, in paragraph [0025]:

Referring to Figure 5, a method in accordance with an embodiment of the present invention is shown. First, the system determines whether the configuration vector representing the optimal performance for a particular application is known (step 200). If so, the vector is retrieved (step 212), the programmable memory module ~~(106)~~ (104) is programmed (step 214), and the application is executed with the optimal memory configuration for that application (step 216).